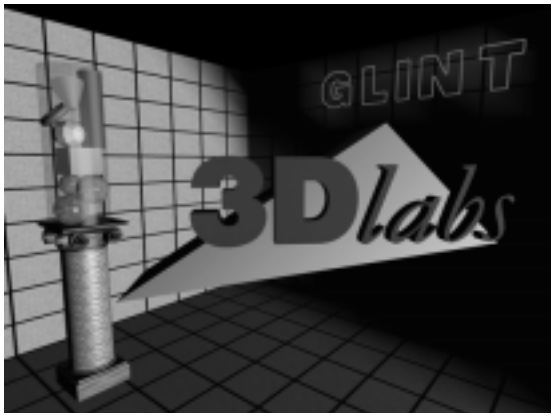
3Dlabs®

GLINT® Delta

Hardware Reference Manual



Issue 4

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Change History

Document	Issue	Date	Change
100.8.0	1.0	28 Nov 95	Creation from Pin Information 1.5 plus electrical data
100.8.0	1.1	6 Feb 96	Updated with Configuration and Control Registers
100.8.0	1.2	15 Feb 96	New address for 3Dlabs Inc.
100.8.0	4	29 July 96	Errata DLEN015 incorporated resulting in changes to section 5.4. Document standardization.

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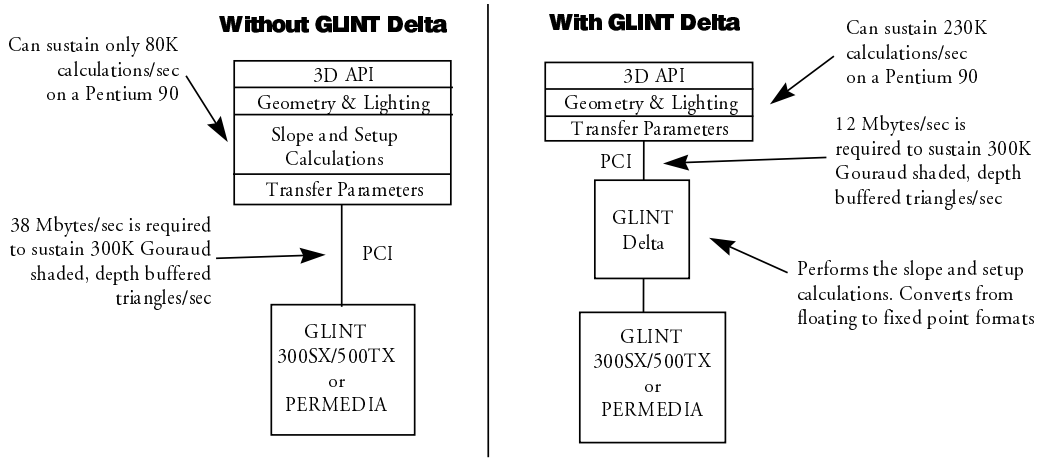
1. Introduction

This document has been written as the reference for hardware and system designers who wish to develop hardware or software using the GLINT® Delta floating point setup processor. A familiarity with the functionality of the GLINT or PERMEDIA rendering devices is assumed in this document.

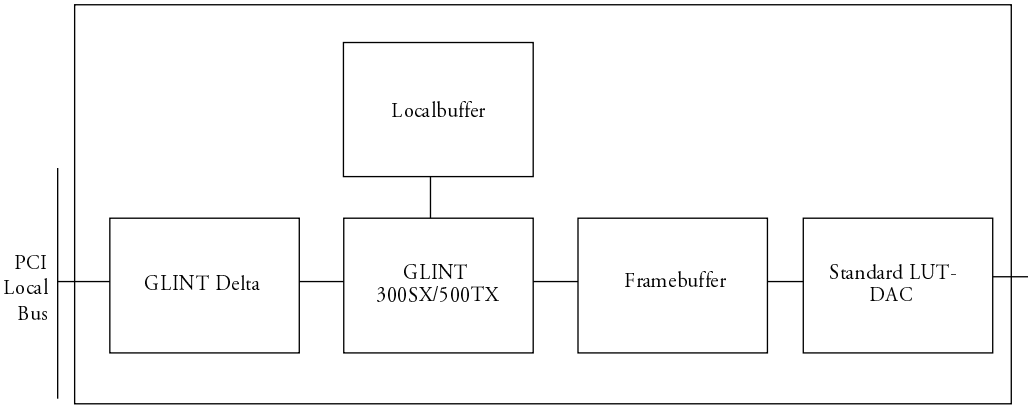
1.1 What is the GLINT Delta?

The GLINT Delta is a 80 MFLOPS setup processor, designed to break the 3D geometry bottleneck on PCs. GLINT Delta calculates the slope and setup information for any 3Dlabs rendering device, e.g. GLINT 300SX/500TX or PERMEDIA. By performing high precision floating point to fixed point conversion, GLINT Delta allows the software geometry pipeline to pass vertex information in standard floating point format.

Coupling GLINT Delta with a 3Dlabs' rendering device can typically double system performance while significantly reducing the load on the CPU and the PCI bus. The setup calculations are general purpose and may be used to accelerate any 3D API, including OpenGL, Direct3D, AutoDesk's Heidi and Apple's QuickDraw 3D.



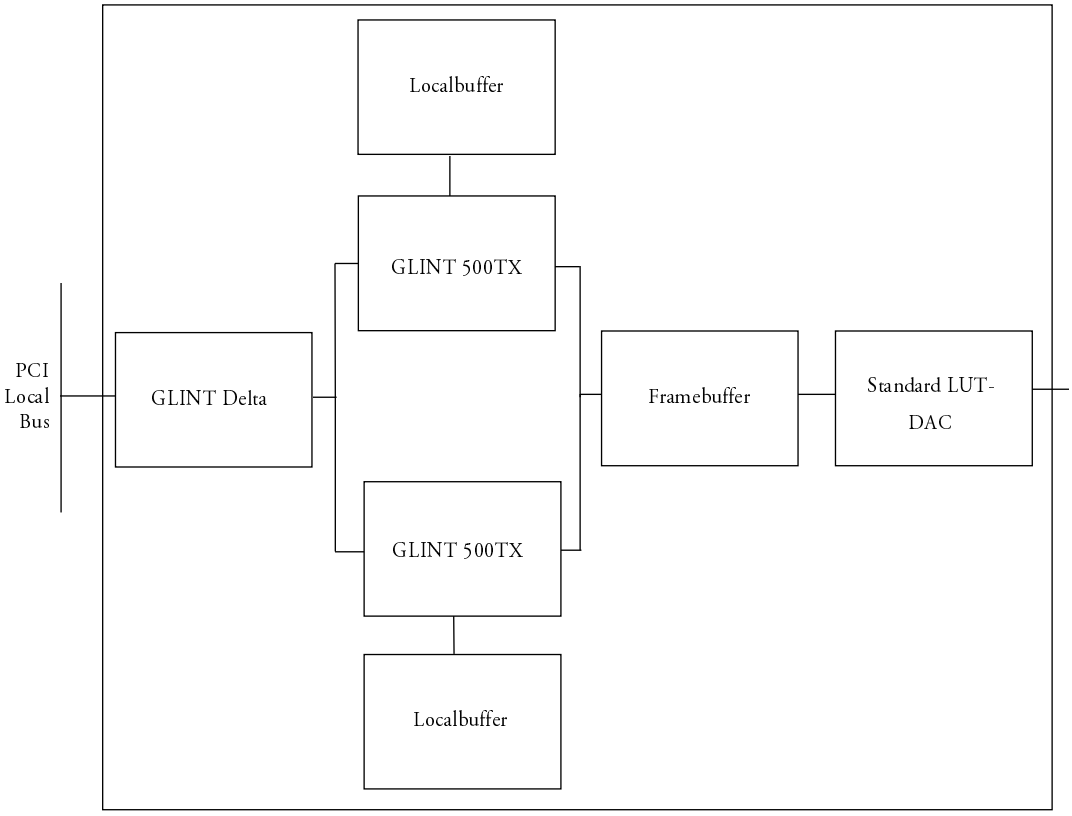
The GLINT Delta contains two on-chip PCI Local Bus interfaces: the primary interface communicates with the host processor and the secondary interface communicates with other PCI devices such as GLINT 300SX/500TX, PERMEDIA or a AVGA device.



A complete 3D/GUI accelerator using GLINT Delta

GLINT Delta functions as a PCI to PCI multi-function adaptor. So, in addition to calculating the slope and setup information, the GLINT Delta can act as a bridge between the PCI bus and multiple graphics devices. This capability may be used in various ways:

- Driving dual GLINT 500TX devices for increased rendering speed;
- Driving a GLINT rendering device plus an AVGA device for 3D acceleration with on-board VGA.



A dual GLINT 500TX accelerator using GLINT Delta

1.2 The GLINT and PERMEDIA Families

The GLINT 300SX and 500TX graphics processors provide 100% OpenGL compliant rendering combined with state-of-the-art Windows acceleration. VRAM framebuffer support enables the high screen resolutions required by professional applications such as CAD and visualization.

The PERMEDIA graphics processor provides high quality 3D, Windows, Video and SVGA acceleration in a single device. Supporting low-cost SGRAM framebuffers, PERMEDIA accelerates a broad range of pervasive multimedia applications including games, animation authoring and Web browsers.

The GLINT Delta is a completely compatible with all the 3Dlabs' rendering devices providing a glueless hardware interface to the GLINT 300SX, GLINT 500TX and PERMEDIA devices. The GLINT Delta programming model is fully compatible with the other GLINT and PERMEDIA devices.

1.3 GLINT Delta Graphics Acceleration

The GLINT Delta adds extra 3D graphics acceleration to the 3Dlabs' rendering devices by implementing the slope and setup calculations for triangles and lines in hardware. Offloading these calculations from the host processor typically doubles 3D system performance. The processing required on the host is greatly reduced and much less data is passed from the host to the graphics subsystem.

1.3.1 Delta Unit

The Delta Unit in the GLINT Delta implements the slope calculations and data conversion for graphics primitives in one unit. This unit can be considered as being positioned in front of the rasterizer in the GLINT 300SX/500TX or PERMEDIA pipelines.

The GLINT Delta accepts the coordinates of vertices plus color, depth, fog and texture parameters. The Delta Unit calculates the parameters required by the GLINT 300SX/500TX or PERMEDIA. GLINT Delta will accept the input parameters in either fixed point format or IEEE single precision floating point format. Internal calculations in GLINT Delta are performed in floating point format. Vertex sharing for meshes, fans and polylines is supported with the shared vertices only being loaded once.

An optional normalize operation may be applied to texture parameters. This operation calculates the maximum absolute value of the texture parameters for a primitive and normalizes all the texture parameters to lie in range -1.0 to 1.0. Normalizing the texture parameters ensures that maximum accuracy is achieved by the texture unit in the GLINT 500TX and PERMEDIA.

The operations in the Delta Unit remove a considerable amount of work from the host processor. However since the transformation and lighting calculations are still performed by software on the host processor, GLINT Delta is able to support all the widely available 3D graphics APIs.

2. PCI Configuration Region

The PCI Configuration Region provides at set of 'hooks' which satisfies the needs of current and anticipated system configuration mechanisms. The configuration registers are accessed and modified by the use of Configuration Read and Write commands.

As GLINT Delta is a multi-function device, the configuration space is split into eight 256 bytes blocks. GLINT Delta has one internal function and up to 2 external functions. The order of the functions as seen by the PCI interface is dependent on whether external function 1 is a VGA device, i.e.

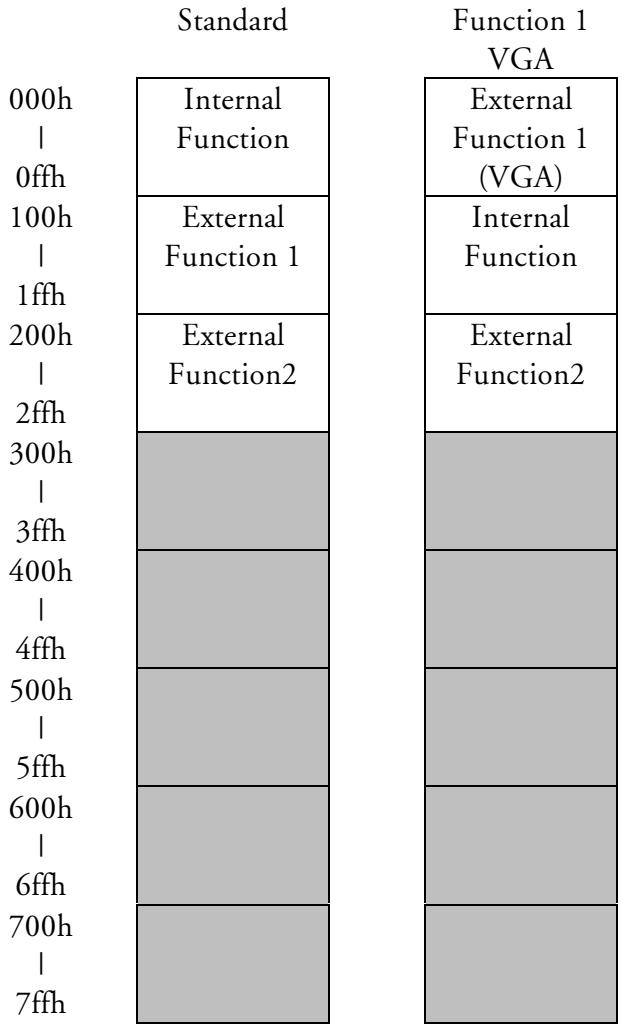


Figure 2-1 Configuration Region Address Map

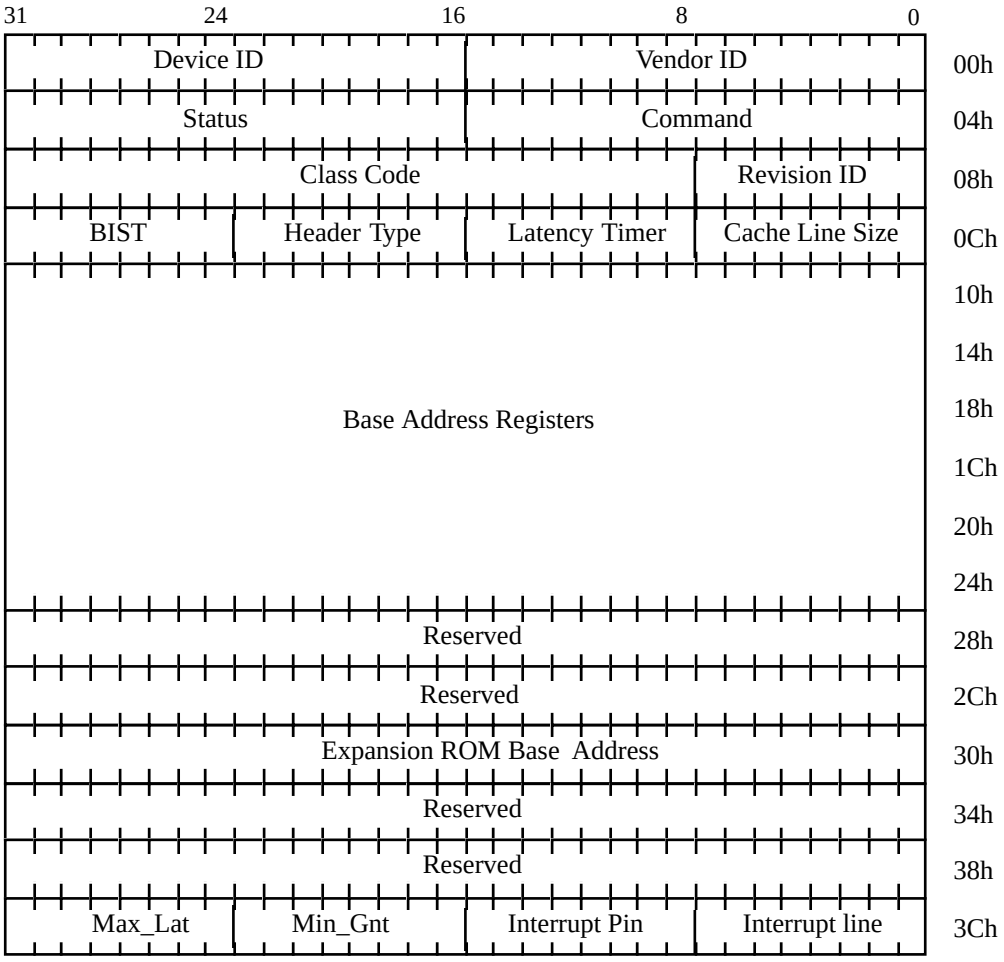
GLINT Delta will only respond to configuration space accesses for which devices exist. Hardware mode pins are used to indicate which of the external functions are populated in

the system. A mode pin is used to indicate that external function 1 is a VGA device. These mode pins are described in section 5.4.

2.1 Internal Function Configuration Registers

64 bytes of the Configuration registers are predefined within the PCI Specification and are supported by GLINT Delta. The remaining 192 Bytes are device specific and are unused by GLINT Delta, returning the value zero.

Table 2-1 Configuration Region.



2.1 Device Identification

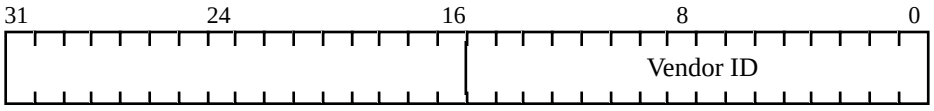
2.1.1 Vendor ID

Vendor identification number.

CFGVendorId

Region: Config **Offset:** 00h

Read Only **Reset Value:** 3D3D



Bits 15-0 **3D3Dh**

3Dlabs company code

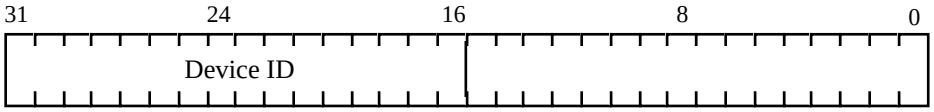
2.1.2 Device ID

Device identification number.

CFGDeviceId

Region: Config **Offset:** 02h

Read Only **Reset Value:** 0003h



Bits 31-16 **0003h**

GLINT Delta Device number

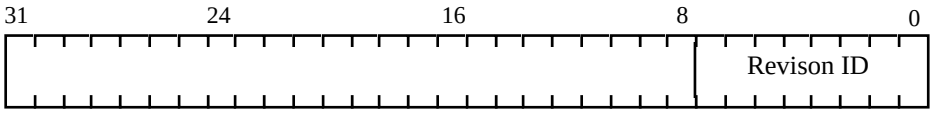
2.1.3 Revision ID

Revision identification number.

CFGRevisionId

Region: Config **Offset:** 08h

Read Only **Reset Value:** Revision Number



The revision ID register returns the following code:

Bits 7 - 0 **Revision**

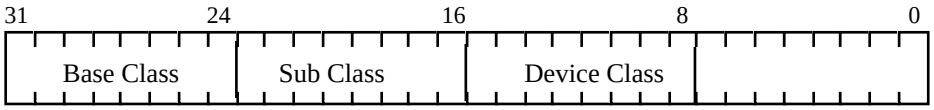
01h = Revision R01

2.1.4 Class Code Register

CFGClassCode

Region: Config **Offset:** 09h

Read Only **Reset Value:** 038000h



Bits 31-24 **03h**

Base class. PCI Definition: Display controller

Bits 23-16 **80h**

Sub class. PCI Definition: Other Display controller (not VGA or XGA)

Bits 15-8 **00h**

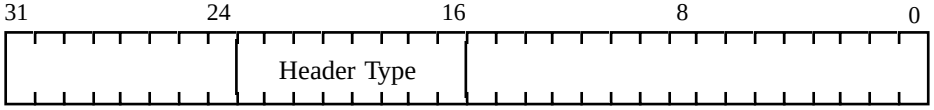
Device class

2.1.5 Header Type

CFGHeaderType

Region: Config **Offset:** 0Eh

Read Only **Reset Value:** 80h



Bits 23-16 **80h**

Header Type. PCI Definition: Multi- function device

2.2 Device Control

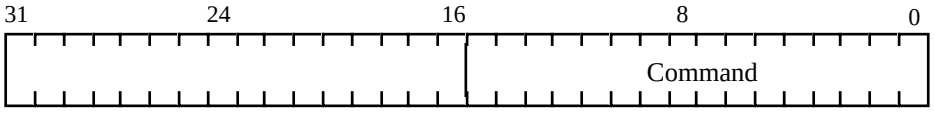
2.2.1 Command Register

The command register provides control over a ability of a device to generate and respond to PCI cycles. Writing zero to this register disconnects the device from the PCI for all except configuration accesses. All necessary bits within the command register are supported for the functionality contained in GLINT Delta.

CFGCommand

Region: Config **Offset:** 04h

Read/Write **Reset Value:** 0000h



Bit 0 **I/O access enable** **(Read Only)**

0 = GLINT Delta has no I/O space regions

Bit 1 **Memory access enable**

0 = Disable memory space accesses. (RESET)

1 = Enable memory space accesses

Bit 2 **Master enable**

0 = Disable master accesses. (RESET)

1 = Enable master accesses

Bit 3 **Special Cycle access enable** **(Read Only)**

0 = GLINT Delta never responds to special cycle accesses.

Bit 4 **Memory Write and Invalidate enable** **(Read Only)**

0 = GLINT Delta master never issues Memory Write and Invalidate accesses.

Bit 5 **VGA palette snoop enable** **(Read Onl)**

0 = GLINT Delta is not a VGA device.

Bit 6 **Parity error report enable** **(Read Only)**

0 = GLINT Delta does not report parity errors.

Bit 7 **Address/Data stepping enable** **(Read Only)**

0 = GLINT Delta does not do stepping.

Bit 8 **SERR driver enable** **(Read Only)**

0 = GLINT Delta does not report parity errors.

Bit 9 **Master Fast back-to-back enable** **(Read Only)**

0 = The GLINT Delta master does not implement fast back-to-back accesses.

Bits 15-10 **Reserved**

000000b

2.3 Device Status

2.3.1 Status Register

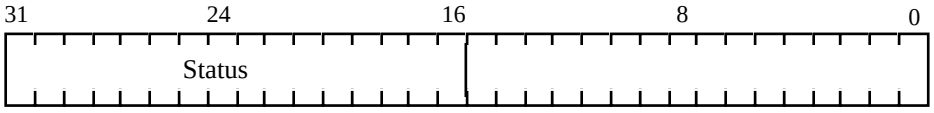
The Status Register is used to record status information for PCI related events. The definition for each bit is given below.

Reads to this register behave normally. Writes function differently in that bits can be reset but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

CFGStatus

Region: Config **Offset:** 06h

Read Only **Reset Value:** 00h



Bits 22-16 **Reserved** **(Read Only)**

0000000b.

Bit 23 **Fast back-to-back Transactions** **(Read Only)**

1 = Indicates support for fast back-to-back PCI transactions .

Bit 24 **Master Parity check flag** **(Read Only)**

0 = Parity checking not implemented on GLINT Delta.

Bits 26-25 **10b** **(Read Only)**

Indicates that GLINT Delta asserts DevselN at medium speed.

Bit 27 **Target Abort flag** **(Read Only)**

0 = GLINT Delta never issues a target abort.

Bit 28 **Master Target Abort flag**

Set by master when transaction terminates with target abort.

Bit 29 **Master Abort flag**

Set by master when it terminates transaction with master abort.

Bit 30 **SERR flag** **(Read Only)**

0 = Parity checking not implemented on GLINT Delta.

Bit 31 **PERR flag** **(Read Only)**

0 = Parity checking not implemented on GLINT Delta.

2.4 Miscellaneous Functions

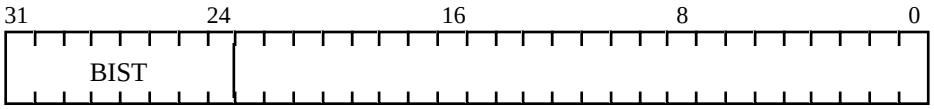
2.4.1 BIST

Optional register used for control and status of BIST.

CFGBist

Region: Config **Offset:** 0Fh

Read Only **Reset Value:** 00h



Bits 31-24 BIST **(Read only)**

00h. BIST unsupported by GLINT Delta over the PCI interface.

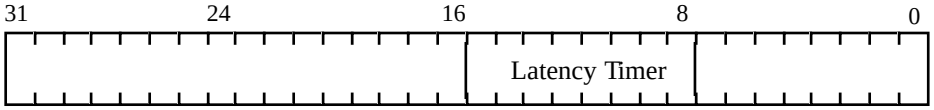
2.4.2 Latency Timer

This register specifies, in PCI bus clocks, the value of the Latency Timer for this PCI bus master.

CFGLatTimer

Region: Config **Offset:** 0Dh

Read/Write **Reset Value:** 00h



Bits 15-8 Latency Timer Count

Sets the maximum number of PCI clock cycles for master burst accesses.

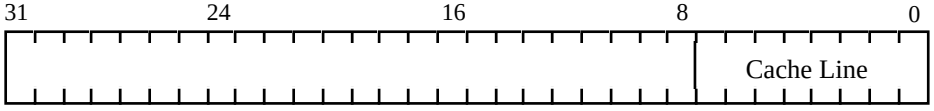
2.4.3 Cache Line Size

This register specifies the cache line size in units of 32 bit words. It is only implemented for masters which use the 'Memory write and invalidate' command. GLINT Delta does not use this command.

CFGCacheLine

Region: Config **Offset:** 0Ch

Read Only **Reset Value:** 00h



Bits 7-0 Cache Line Size

00h. Cache line size unsupported.

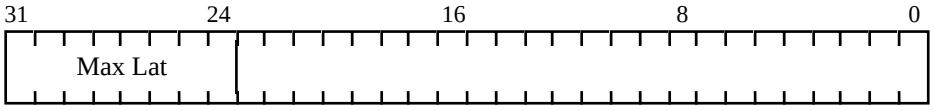
2.4.4 Maximum Latency

This register specifies how often the PCI device needs to gain access to the PCI bus.

CFGMaxLat

Region: Config **Offset:** 3Fh

Read Only **Reset Value:** 80h



Bits 31-24 Maximum Latency **(Read only)**

80h.

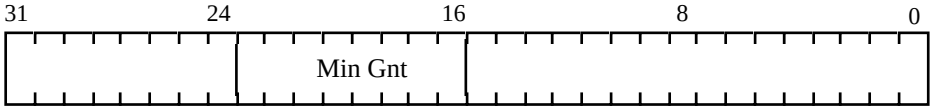
2.4.5 Minimum Grant

This register specifies how long a burst period the PCI device needs.

CFGMinGrant

Region: Config **Offset:** 3Eh

Read Only **Reset Value:** 80h



Bits 23-16 Minimum Grant **(Read only)**

80h.

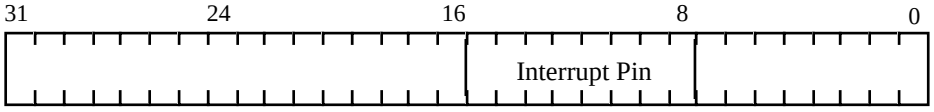
2.4.6 Interrupt Pin

The Interrupt Pin register tells the BIOS which interrupt line GLINT Delta uses.

CFGIntPin

Region: Config **Offset:** 3Dh

Read Only **Reset Value:** 01h



Bits 15-8 Interrupt Pin

01h GLINT Delta uses Interrupt pin A

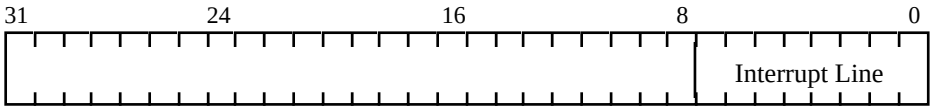
2.4.7 Interrupt Line

The Interrupt Line register is an 8 bit register used to communicate interrupt line routing information.

CFGIntLine

Region: Config **Offset:** 3Ch

Read/Write **Reset Value:** 00h



Bits 7-0 **Interrupt Line**

2.5 Base Addresses

The base address registers allow the boot software to relocate PCI devices in the address spaces. At system power-up device independent software must be able to determine which devices are present, build a consistent address map, and determine if a device has an expansion ROM. GLINT Delta has just one region. All other Base address registers are read only and return the value 0000.0000h. GLINT Delta does not have an expansion ROM and so the expansion ROM base address is also read only, returning the value 0000.0000h.

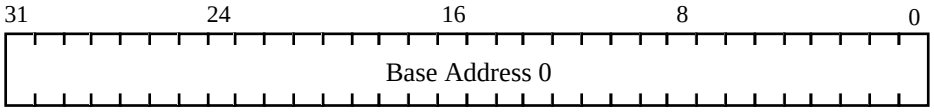
2.5.1 Base Address 0 Register

The Base Address 0 Register contains the GLINT Delta control space offset. The control registers are in memory space. They are not prefetchable and can be located anywhere in 32 bit address space.

CFGBaseAddr0

Region: Config **Offset:** 10h

Read/Write **Reset Value:** 0000.0000h



Bits 31-17 **Base offset**

Loaded at boot time to set offset of the control register space.

Bits 16-4 **Size indication** **Read Only**

000h Indicates that the control registers must be mapped into 128 KBytes.

Bits 3-0 **Address Type** **Read Only**

0h Memory Space, not prefetchable, in 32 bit address space

3. Region 0 - Control Registers

3.1 Region 0 Address Map

The GLINT Delta region 0 is a 128 KByte region containing the control registers and ports to and from the GLINT and PERMEDIA Graphics Core.

The 64 Kbyte control space is mapped twice in the 128 KByte region. The lower 64 Kbyte region is for access by little-endian processors. The top 64 Kbytes includes byte swapping for big-endian processors.

The control register space is partitioned as follows:

Offset	Function	Byte Swap Offset
0000.0000h - 0000.0FFFh	Control Status Registers	0001.0000h - 0001.0FFFh
0000.1000h - 0000.17FFh	Localbuffer Registers	0001.1000h - 0001.17FFh
0000.1800h - 0000.1FFFh	Framebuffer Registers	0001.1800h - 0001.1FFFh
0000.2000h - 0000.2FFFh	GC FIFO Interface	0001.2000h - 0001.2FFFh
0000.3000h - 0000.3FFFh	Internal Video Registers	0001.3000h - 0001.3FFFh
0000.4000h - 0000.7FFFh	External Video Registers	0001.4000h - 0001.7FFFh
0000.8000h - 0000.FFFFh	GC Register Access (Through FIFO)	0001.8000h - 0001.FFFFh

Figure 3-1 Region 0 Address Map

3.2 Control Status Registers

The GLINT Delta Control Status Register region is split into two sections. The lower section allows direct access to the control status registers of the GLINT or PERMEDIA rendering device connected to GLINT Delta. Some of the registers in this section are actually GLINT Delta registers which are shadowing GLINT 300SX/500TX or PERMEDIA operations for software compatibility with systems without GLINT Delta.

The upper section has additional GLINT Delta registers which are documented below. Refer to the appropriate GLINT 300SX/500TX or PERMEDIA Hardware Reference Manual for details on registers in the lower region.

3.2.1 Reset Status Register

Writing to the reset status register forces a software reset of the GLINT Delta Graphics Core. The software reset does not reset the GLINT Delta primary PCI interface. It is provided for software diagnostics in case an incorrect register set up locks up the GLINT Delta internal GC.

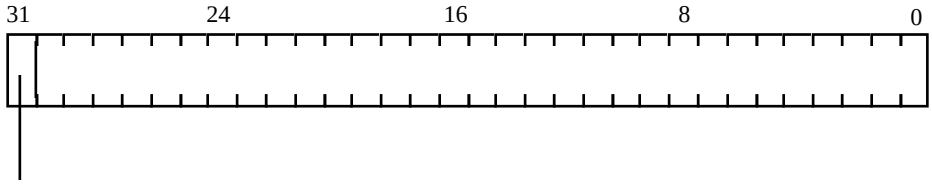
The software reset takes a number of cycles and the GC must not be used during the reset. A flag in the register is provided which shows that the software reset is still in progress.

For more information on the operation of the GLINT Delta at reset. Various mode pins are sampled at reset, these pins are described in section 5.4.

DResetStatus

Region: 0 **Offset:** 0000.0800h

Read/Write **Reset Value:** 0000.0000h



Software Reset Flag

Bits 30-0 **Reserved**

Bit 31 **Software Reset Flag**

0 = GLINT Delta is ready for use
1 = GLINT Delta is being reset and must not be used

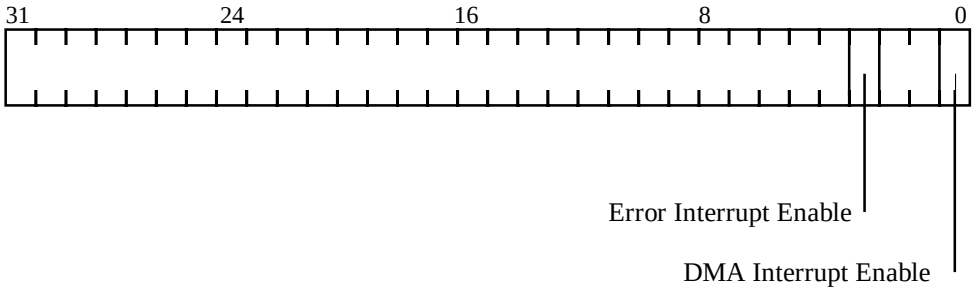
3.2.2 Interrupt Enable Register

The Interrupt Enable Register allows for a number of GLINT Delta flags to generate a PCI interrupt. Two interrupt sources are defined below. At reset all interrupts sources are disabled.

DIntEnable

Region: 0 **Offset:** 0000.0808h

Read/Write **Reset Value:** 0000.0000h



Bit 0 **DMA interrupt enable**

0 = Disable interrupt (RESET)
1 = Enable interrupt

Bit 3 **Error interrupt enable**

0 = Disable interrupt (RESET)
1 = Enable interrupt

The conditions which cause the above interrupts to be generated are described in section 3.2.3.

3.2.3 Interrupt Flags Register

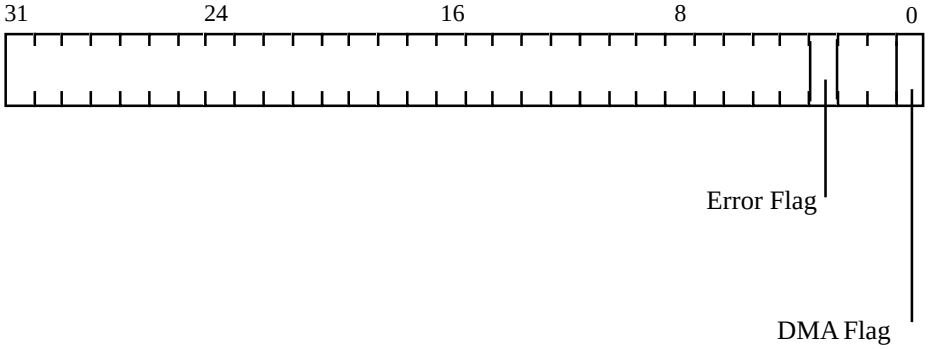
The Interrupt Flags Register shows which interrupts are outstanding on GLINT Delta.

Flag bits are reset by writing to this register with the corresponding bit set to a 1. Flags at positions where the bits are set to 0 will be unaffected by the write.

DIntFlags

Region: 0 **Offset:** 0000.0810h

Read/Write **Reset Value:** 0000.0000h



Bit 0 **DMA Flag**

0 = No interrupt (RESET)
1 = Interrupt outstanding

Bit 3 **Error Flag**

0 = No interrupt (RESET)
1 = Interrupt outstanding

The DMA flag is set on the completion of a DMA transfer.

The Error Flag is set for the following error conditions:

1) Input FIFO error. The GLINT Delta input FIFO has been written to when full. The data is discarded and this error flag is set. N.B. If input FIFO disconnect is enabled, then this flag will never be set as the GLINT Delta will stop the FIFO from overfilling.

2) DMA Error. The GLINT Delta input FIFO has been written to while a DMA transfer was in process. The data in the input FIFO becomes corrupt and hence subsequent GLINT Delta operations are indeterminate.

3.2.4 Error Flags Register

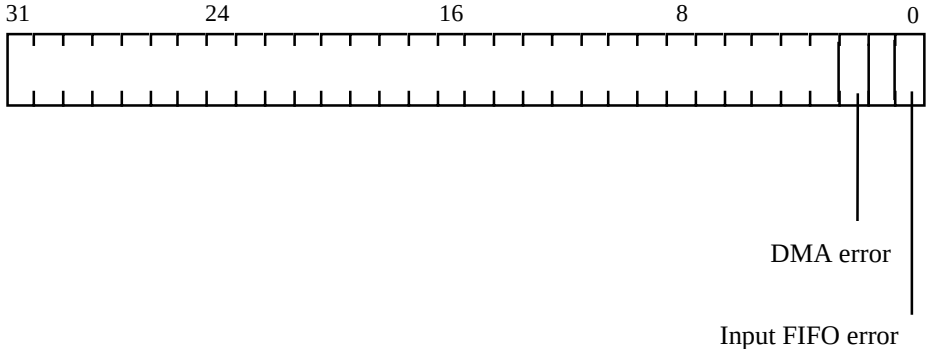
The Error Flags Register shows which errors are outstanding on GLINT Delta.

Flag bits are reset by writing to this register with the corresponding bit set to a 1. Flags at positions where the bits are set to 0 will be unaffected by the write.

DErrorFlags

Region: 0 **Offset:** 0000.0838h

Read/Write **Reset Value:** 0000.0000h



Bit 0 **Input FIFO Error Flag**

Flag set on write to full input FIFO

0 = No error (RESET)

1 = Error outstanding

Bit 2 **DMA Error Flag**

Flag set on write to input FIFO when DMA in operation

0 = No error (RESET)

1 = Error outstanding

3.2.5 Test Register

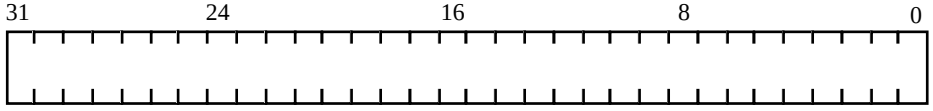
The test register is not to be used by any user software. Writes to this register have an undefined effect.

The GLINT Delta powers up in functional mode.

DTestRegister

Region: 0 **Offset:** 0000.0848h

Read/Write **Reset Value:** 0000.0000h



3.2.6 FIFO Disconnect Register

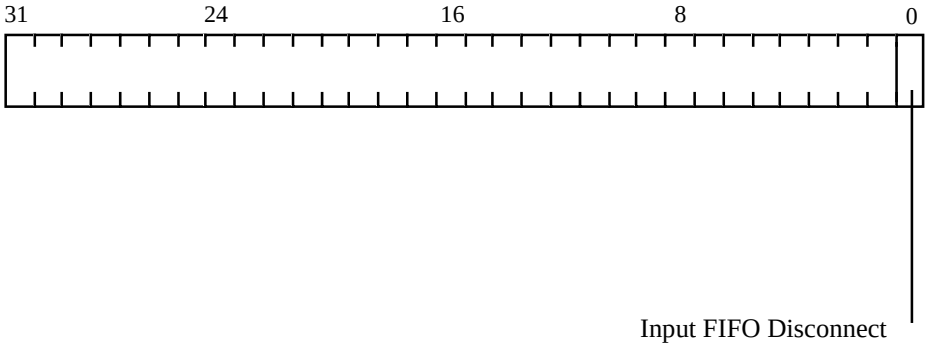
The FIFO Disconnect Register enables input FIFO disconnect on GLINT Delta.

Disconnect is disabled at reset.

DFIFODis

Region: 0 **Offset:** 0000.0868h

Read/Write **Reset Value:** 0000.0000h



Bit 0 **Input FIFO Disconnect enable**

0 = Disabled (RESET)
1 = Enabled

3.3 Localbuffer Registers

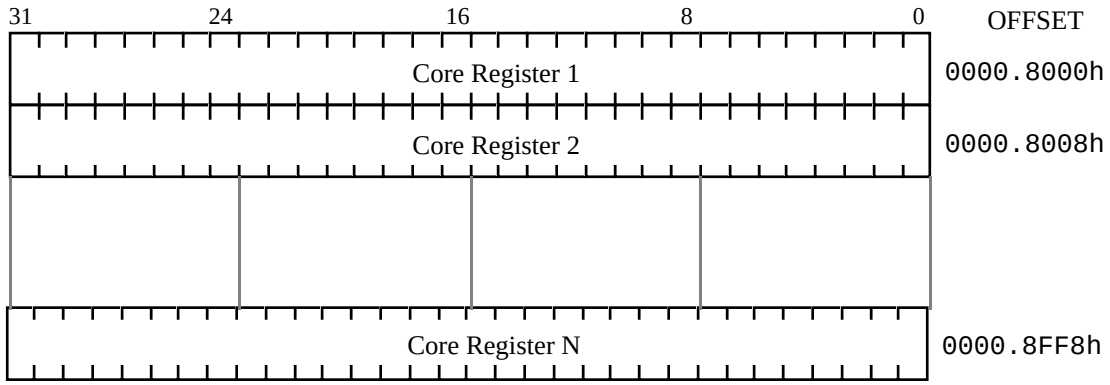
Refer to GLINT 300SX/500TX or PERMEDIA Hardware Reference Manuals.

3.4 Framebuffer Registers

Refer to GLINT 300SX/500TX or PERMEDIA Hardware Reference Manuals.

3.5 Graphics Core Registers

All the Graphics Core registers in the GLINT Delta, GLINT 300SX/500TX and PERMEDIA are addressed in this part of region 0. The address for each register and associated data fields is defined in the appropriate Programmers Reference Manual.



Note. Not all the available register locations are used within the Graphics Core. The registers are on 64 bit boundaries.

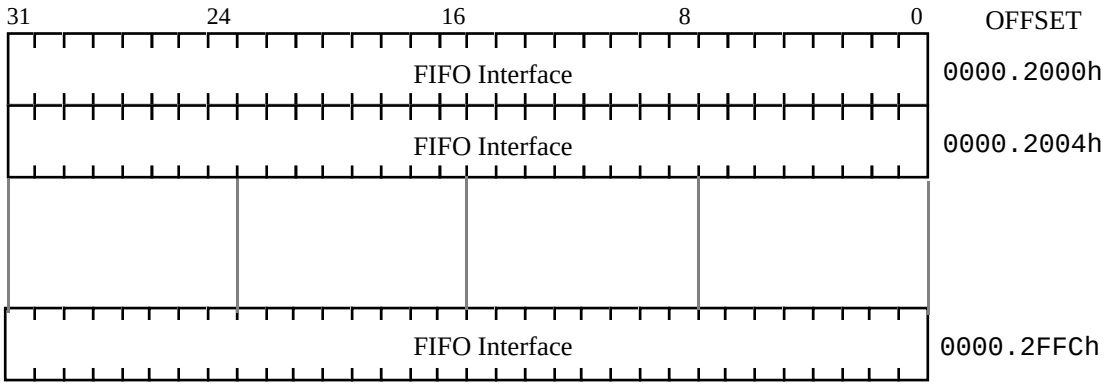
3.6 Graphics Core FIFO Interface

The Graphics Core FIFO interface provides a port through which both GC register addresses and data can be sent to the input FIFO. A range of 4 KBytes of host space is provided although all data may be sent through one address in the range. ALL accesses go directly to the FIFO, the range is provided to allow for data transfer schemes which force the use of incrementing addresses. Before writing to the input FIFO the user must check that there is sufficient space by reading the InFIFOSpace register.

If the FIFO interface is used, then data is typically sent to the GLINT Delta in pairs, an address word which addresses the register to be updated, followed by the data to be sent to the register. Note that the GC registers can not be read through this interface. Command buffers generated to be sent to the input FIFO interface may be read directly by the GLINT Delta by using the DMA controller.

A data formatting scheme is provided to allow for multiple data words to be sent with one address word where adjacent or grouped registers are being written, or where one register is to be written many times.

For more information on the direct FIFO interface data buffer formats please refer to the GLINT Delta, GLINT 300SX/500TX and PERMEDIA Programmers Reference Manuals.



Note. The FIFO interface can be accessed at 32 bit boundaries. This is to allow a direct copy from a DMA format buffer.

4. Electrical Data

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Junction Temperature	100°C
Storage Temperature	-65°C to 150°C
DC Supply Voltage	3.8V
I/O Pin Voltage with respect to GND	-0.5V to 5.5V

4.2 DC Specifications

Table 4-2 DC Specifications

Symbol	Parameter	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
L_{PIN}	Pin Inductance		18.4	nH
I_{CC}	Power Supply Current		500	mA

Table 4-3 PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{PIL}	Input Low Voltage		Note 1	V
V_{PIH}	Input High Voltage	Note 1		V
V_{POL}	Output Low Voltage		0.5	V
V_{POH}	Output High Voltage	2.4		V
I_{PIL}	Input Low Current		Note 1	mA
I_{PIH}	Input High Current		Note 1	mA
C_{PIN}	Input Capacitance		10	pF
C_{CLK}	PCI Clock Input Capacitance		12	pF
C_{IDSEL}	PCI Idsel Input Capacitance		8	pF

Note 1: This value is PCI 2.1 compliant

4.3 AC Specifications

Table 4-4 Test Loads for AC Timing

Pin Name	Capacitive Load
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN,PCIIntAN, SCIAD[31:0], SCICBEN[3:0], SCIPar, SCIFrameN[1:0],SCIIRdyN[1:0], SCITRdyN[1:0],SCIStopN[1:0], SCIDevselN[1:0].	50pF
SCIClkOut[3:0],PCIFIFOInDis.	20pF

4.3.1 Clock Timing

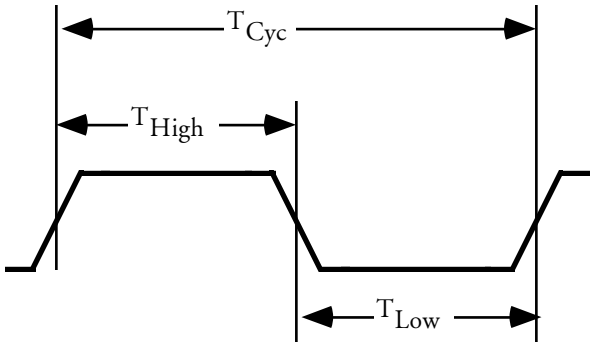


Figure 4-1 Clock Waveform Timing

Table 4-5 Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time	30		nS	
T_{PHigh}	PCIClk High Time	11		nS	
T_{PLow}	PCIClk Low Time	11		nS	
T_{MCyc}	MClk Cycle Time	30	50	nS	
T_{MHigh}	MClk High Time	10		nS	
T_{MLow}	MClk Low Time	10		nS	
T_{SCyc}	SCIClk Cycle Time	30		nS	
T_{SHigh}	SCIClk High Time	10		nS	
T_{SLow}	SCIClk Low Time	10		nS	

4.3.2 Input / Output Timing

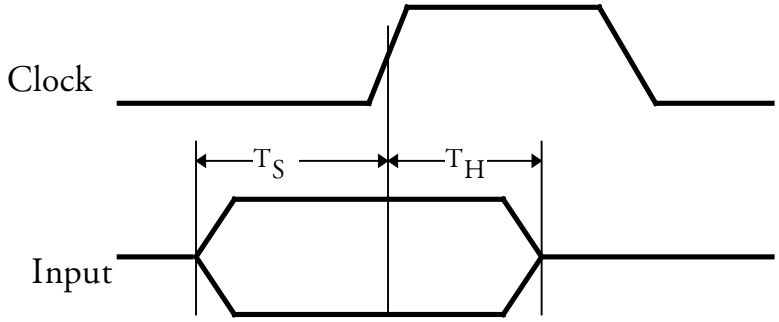


Figure 4-2 Clock Referenced Input Timing

Table 4-6 PCIClk Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units	Notes
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	7	0	nS	
PCIGntN	10	0	nS	
PCIRstN	7	0	nS	1

Notes:

1. PCIRstN is resynchronised internally. The given timings, when met, ensure that the reset is detected in the current cycle.

Table 4-7 SCIClk Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units	Notes
SCIAD(31:0), SCICBEN(3:0), SCIPar, PCIIRdyN(1:0), PCITRdyN(1:0), PCIStopN(1:0), PCIDevselN(1:0), GLINTInDis(1:0)	10	0.2	nS	
ModeCtl(1:0), VGAEn, ExtFuncEn(1:0)	10	2	nS	

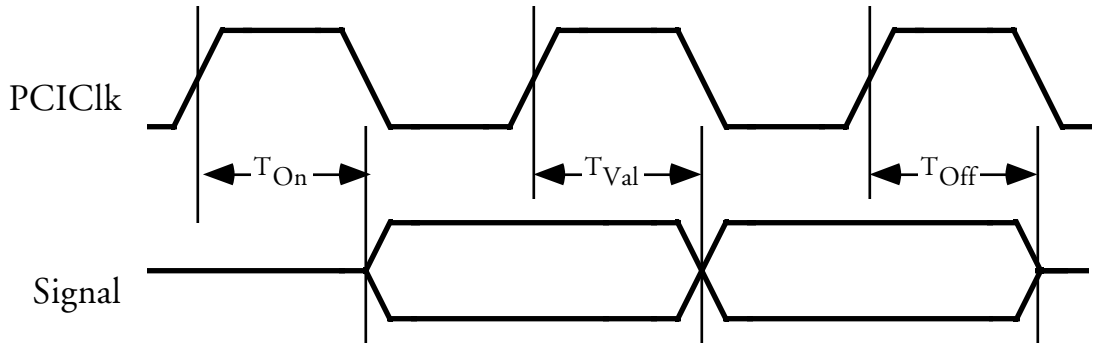


Figure 4-3 PCIClk Referenced Output Timing

Table 4-8 PCIClk Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	2	11	2	11	2	11	nS	
PCIReqN	2	12					nS	
PCIIntAN	2	15					nS	1

Notes:

1. Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

5. Pin Information

5.1 Package Pinout

The GLINT Delta comes in a 176 pin PQFP package. The pin numbering is shown in figure 5-1.

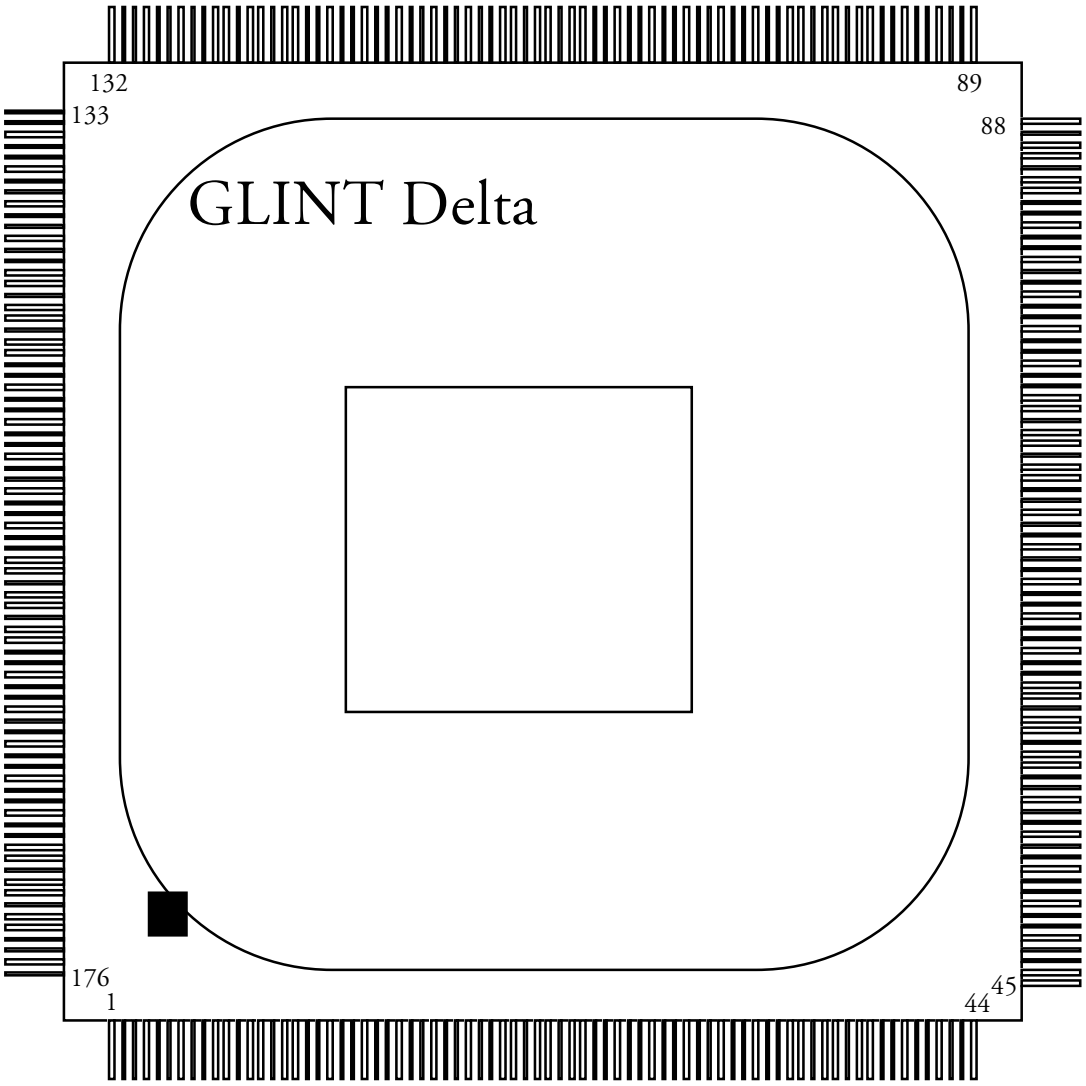


Figure 5-1 GLINT Delta Pin Numbering

5.2 Pin Descriptions

Table 5-1 provides a brief description of each pin. The following pin type definitions are used:

I	Input signal
O	Output signal
I/O	Bi-directional signal
OD	Open drain output
P	PCI compatible output
NC	No connect

Table 5-1 Pin Descriptions

Symbol	Type	Power	Pin Number(s)	Description
Clocks				
PCIClk	I		170	PCI clock.
MClk	I		126	System clock. Used for all internally clocked functions on the chip.
SCIClk	I		139	SCI clock.
SCIClkOut(3:0)	O	P	156-159	SCI clock drivers.
PCI Interface				
PCIRstN	I		162	Power On and Hardware reset.
PCIAD(31:0)	I/O	P	165,171,173-175, 1-3,7,11-13,15-17, 19,31,33-35,38-40, 42,44,46,47,49-51, 54,55	PCI Address and Data bus.
PCICBEN(3:0)	I/O	P	5,20,30,43	PCI command and bytes enables.
PCIPar	I/O	P	29	PCI parity bit.
PCIFrameN	I/O	P	21	PCI frame control line.
PCIIRdyN	I/O	P	24	PCI Initiator Ready.
PCITRdyN	I/O	P	25	PCI Target Ready.
PCIStopN	I/O	P	28	PCI Target Stop control.
PCIIdsel	I		6	PCI slot configuration select line.
PCIDevselN	I/O	P	26	PCI Target selected.
PCIReqN	O	P	167	PCI Master request line.
PCIGntN	I		166	PCI Master Grant line.
PCIIntAN	OD	P	161	PCI interrupt line.
PCIFIFOInDis	O	P	144	PCI disconnect

Table 5-1 Pin Descriptions (Continued)

Symbol	Type	Power	Pin Number(s)	Description
SCI Interface				
SCIRstN	O	P	123	Secondary bus reset.
SCIAD(0:31)	I/O	P	56,58-61,63-65,69, 70,72-75,77,78, 104,105,116-119, 121,122,129, 131-134,136,137, 143	SCI Address and Data bus.
SCICBEN(0:3)	O	P	68,79,102,128	SCI command and bytes enables.
SCIPar	I/O	P	84	SCI parity bit.
SCIFrameN(0:1)	I/O	P	98,99	SCI frame control lines.
SCIIRdyN(0:1)	I/O	P	92,93	SCI Initiator Ready.
SCITRdyN(0:1)	I		94,95	SCI Target Ready.
SCIStopN(0:1)	I		82,83	SCI Target Stop control.
SCIDevselN(0:1)	I		87,88	SCI Target selected.
ExtFuncEn(0:1)	I		106,108	External function enable lines.
SCIIntAN	I		127	SCI interrupt line.
Misc.				
ModeCtl(0:1)	I		138,142	Reset mode control pins
VGAEn	I		163	VGA enable
GLINTInDis(0:1)	I		146,147	GLINT input FIFO disconnect
TestMode	I		153	Test mode control.
TestAClk	I		151	Test clock A. Internal Pulldown
TestBClk	I		152	Test clock B. Internal Pulldown
TestCClk	I		10	Test clock C. Internal Pulldown
TestGClk	I		150	Test clock G. Internal Pulldown
VDD	I		4,8,18,22,36,41,48, 52,62,66,76,80,96, 110,124,135,140, 145,154,168	Vdd pins. All must be used
GND	I		9,14,23,27,32,37, 45,53,57,67,71,81, 91,97,103,107,109, 111,112,114,120, 125,130,141,155, 160,164,169,172, 176	Ground pins. All must be used.

5.3 Pin Lists

Table 5-2 Alphabetical Pin Listing

Symbol	Pin Numbers
ExtFuncEn(0:1)	106,108
GLINTInDis(0:1)	146,147
GND	9,14,23,27,32,37,45,53,57,67,71,81,91,97,103,107,109,111,112,114,120,125, 130,141,155,160,164,169,172,176
MClk	126
ModeCtl(0:1)	138,142
PCIAD(31:0)	165,171,173-175,1-3,7,11-13,15-17,19,31,33-35,38-40,42,44,46,47,49-51,54,55,
PCICBEN(3:0)	5,20,30,43
PCIClk	170
PCIDevselN	26
PCIFIFOInDis	144
PCIFrameN	21
PCIGntN	166
PCIIdsel	6
PCIIntAN	161
PCIIRdyN	24
PCIPar	29
PCIReqN	167
PCIRstN	162
PCIStopN	28
PCITRdyN	25
SCIAD(0:31)	56,58-61,63-65,69,70,72-75,77,78,104,105,116-119,121,122,129, 131-134,136,137,143
SCICBEN(0:3)	68,79,102,128
SCIClk	139
SCIClkOut(3:0)	156-159
SCIDevselN(0:1)	87,88
SCIFrameN(0:1)	98,99
SCIIntAN	127
SCIIRdyN(0:1)	92,93
SCIPar	84
SCIRstN	123
SCIStopN(0:1)	82,83
SCITRdyN(0:1)	94,95

Table 5-2 Alphabetical Pin Listing (Continued)

Symbol	Pin Numbers
TestAClk	151
TestBClk	152
TestCClk	10
TestGClk	150
TestMode	153
VDD	4,8,18,22,36,41,48,52,62,66,76,80,96,110,124,135,140,145,154,168
VGAEn	163

Table 5-3 Numerical Pin Listing

Pin	Name
1	PCIAD26
2	PCIAD25
3	PCIAD24
4	VDD
5	PCICBEN3
6	PCIIdsel
7	PCIAD23
8	VDD
9	GND
10	TestCClk
11	PCIAD22
12	PCIAD21
13	PCIAD20
14	GND
15	PCIAD19
16	PCIAD18
17	PCIAD17
18	VDD
19	PCIAD16
20	PCICBEN2
21	PCIFrameN
22	VDD

Pin	Name
23	GND
24	PCIIRdyN
25	PCITRdyN
26	PCIDevselN
27	GND
28	PCIStopN
29	PCIPar
30	PCICBEN1
31	PCIAD15
32	GND
33	PCIAD14
34	PCIAD13
35	PCIAD12
36	VDD
37	GND
38	PCIAD11
39	PCIAD10
40	PCIAD9
41	VDD
42	PCIAD8
43	PCICBEN0
44	PCIAD7

Table 5-3 Numerical Pin Listing (Continued)

Pin	Name
45	GND
46	PCIAD6
47	PCIAD5
48	VDD
49	PCIAD4
50	PCIAD3
51	PCIAD2
52	VDD
53	GND
54	PCIAD1
55	PCIAD0
56	SCIAD0
57	GND
58	SCIAD1
59	SCIAD2
60	SCIAD3
61	SCIAD4
62	VDD
63	SCIAD5
64	SCIAD6
65	SCIAD7
66	VDD

Pin	Name
67	GND
68	SCICBEN0
69	SCIAD8
70	SCIAD9
71	GND
72	SCIAD10
73	SCIAD11
74	SCIAD12
75	SCIAD13
76	VDD
77	SCIAD14
78	SCIAD15
79	SCICBEN1
80	VDD
81	GND
82	SCIStopN0
83	SCIStopN1
84	SCIPar
85	NC
86	NC
87	SCIDevselN0
88	SCIDevselN1

Table 5-3 Numerical Pin Listing (Continued)

Pin	Name
89	NC
90	NC
91	GND
92	SCIIRdyN0
93	SCIIRdyN1
94	SCITRdyN0
95	SCITRdyN1
96	VDD
97	GND
98	SCIFrameN0
99	SCIFrameN1
100	NC
101	NC
102	SCICBEN2
103	GND
104	SCIAD16
105	SCIAD17
106	ExtFuncEn0
107	GND
108	ExtFuncEn1
109	GND
110	VDD

Pin	Name
111	GND
112	GND
113	NC
114	GND
115	NC
116	SCIAD18
117	SCIAD19
118	SCIAD20
119	SCIAD21
120	GND
121	SCIAD22
122	SCIAD23
123	SCIRstN
124	VDD
125	GND
126	MClk
127	SCIIntAN
128	SCICBEN3
129	SCIAD24
130	GND
131	SCIAD25
132	SCIAD26

Table 5-3 Numerical Pin Listing (Continued)

133	SCIAD27
134	SCIAD28
135	VDD
136	SCIAD29
137	SCIAD30
138	ModeCtl0
139	SCIClk
140	VDD
141	GND
142	ModeCtl1
143	SCIAD31
144	PCIFIFOInDis
145	VDD
146	GLINTInDis0
147	GLINTInDis1
148	NC
149	NC
150	TestGClk
151	TestAClk
152	TestBClk
153	TestMode
154	VDD

155	GND
156	SCIClkOut3
157	SCIClkOut2
158	SCIClkOut1
159	SCIClkOut0
160	GND
161	PCIIntAN
162	PCIRstN
163	VGAEn
164	GND
165	PCIAD31
166	PCIGntN
167	PCIReqN
168	VDD
169	GND
170	PCIClk
171	PCIAD30
172	GND
173	PCIAD29
174	PCIAD28
175	PCIAD27
176	GND

5.4 Pin Description Notes

1. PCIFIFOInDis is currently unused and hence should be left unconnected.
2. The signals SCIFrameN(0:1), SCIIRdyN(0:1), SCITRdyN(0:1), SCIStopN(0:1), SCIDevselN(0:1) and SCIIntAN should all be pulled high regardless of the number of devices fitted to the secondary PCI bus.
3. ModeCtl0 is used for Windows 95 compatibility. If ModeCtl0 is pulled high, then GLINT Delta will override the PCI base and sub class reported by devices on the secondary PCI bus. GLINT Delta and any GLINT rendering device on the secondary PCI bus will have 00h reported as their PCI base class and 00h reported as their PCI sub-class. Any VGA device on the secondary PCI bus will have 00h reported as its PCI base class and 01h reported as its PCI sub-class. These values are required for Windows 95 compatibility. It is recommended that this pin is pulled high.
4. If ModeCtl1 is pulled high, then the PCI Maximum Latency is forced to zero. If ModeCtl1 is pulled low, then the PCI Maximum Latency will be set to 80h.
5. VGAEn is pulled high to indicate that secondary device 0 is a VGA device. If no VGA device is fitted, then this pin should be pulled low.
6. The TestMode pin should be pulled low. The other test pins (TestAClk, TestBClk, TestCClk, TestGClk) may be left unconnected.
7. SCIAD28 should be connected to PCIIdsel of a device fitted as secondary device 0 and SCIAD29 should be connected to PCIIdsel of a device fitted as secondary device 1.
8. GLINTInDis0 should be connected to pin 47 of a GLINT rendering device fitted as secondary device 0 and GLINTInDis1 should be connected to pin 47 of a GLINT rendering device fitted as secondary device 1.
9. If a GLINT rendering device is fitted as secondary device 0, then GLINTInDis0 should be pulled low, otherwise GLINTInDis0 should be pulled high. If a GLINT rendering device is fitted as secondary device 1, then GLINTInDis1 should be pulled low, otherwise GLINTInDis1 should be pulled high.
10. If a device is fitted to secondary device 0, then ExtFuncEn0 should be pulled high, otherwise ExtFuncEn0 should be pulled low. If a device is fitted to secondary device 1, then ExtFuncEn1 should be pulled high, otherwise ExtFuncEn1 should be pulled low.

N.B.

1. A pin should be pulled high by connecting to +5V via a 10K resistor. A pin should be pulled low by connecting to ground via a 10K resistor.

2. Pins marked as NC must NOT be connected.

5.5 Package Dimensions

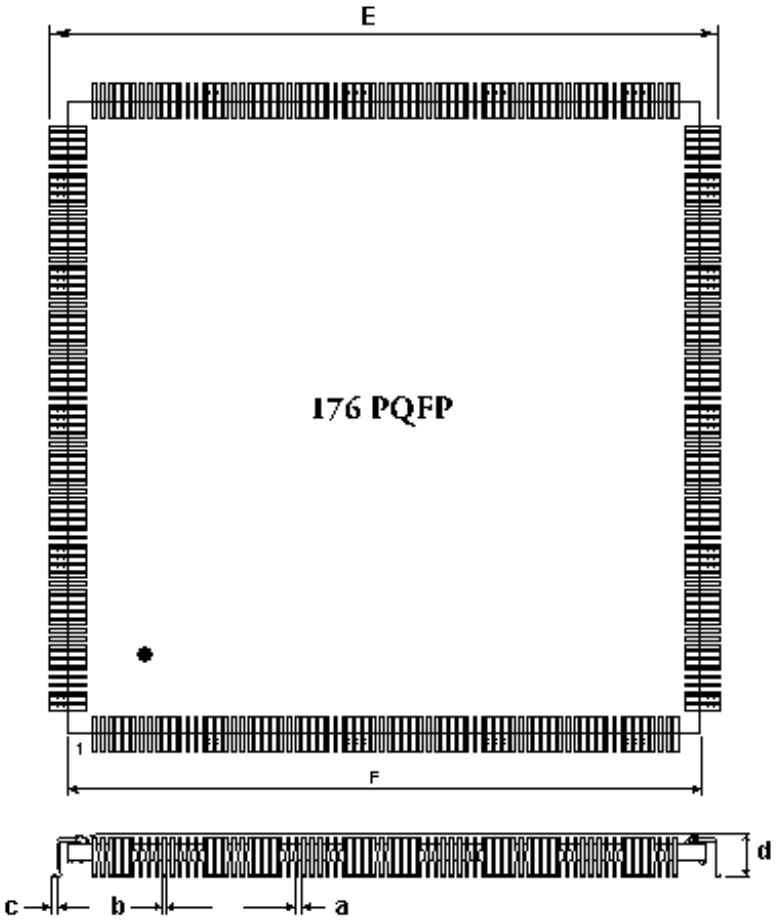


Figure 5-2 Mechanical Diagrams

Table 5-4 176 pin PQFP Package Dimensions

Dimension		mm
a	Lead Pitch	0.5
b	Lead Width	0.22 ± 0.05
c	Foot Length	0.6 ± 0.15
d	Height	1.6 max
E	Width (toe to toe)	26.0
F	Body Width	24.0